Kyoungjoon Ha

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SUMMARY

Circuit design engineer with 3 years of industry experience following an M.S. in integrated circuit design. Architected and implemented RTL for high-speed SerDes interconnect PHYs (UCIe, MIPI D-PHY/C-PHY) at Samsung Electronics, with prior analog research designing transistor-level PLLs (all-digital and injection-locked). Fluent across the analog/digital boundary, from transistor-level circuits to RTL.

EXPERIENCE

Samsung Electronics — Circuit Design Engineer Aug 2023 – Present

Hwaseong, South Korea

Low-Power 32 GT/s x32 Advanced-Package UCIe PHY for Die-to-Die (D2D) Interface

- Led the architecture and RTL design of the Link Training State Machine (LTSM), covering mainband control, analog calibration, and sideband logic for a UCIe-compliant die-to-die Logical PHY.
- Defined PHY initialization and training sequences with the analog team to bring up the 32 GT/s link.
- Integrated digital PHY subsystems over an APB interface and implemented the APB protocol-handling logic for register access and control.
- Owned digital frontend development end to end: RTL simulation, linting, CDC analysis, and synthesis.

MIPI D-PHY / C-PHY

- Developed MIPI digital PHY logic in compliance with the D-PHY and C-PHY specifications.
- Drove the digital backend flow for the digital SerDes, optimizing buffer count via STA-guided ECO in PrimeTime to meet timing closure.

Post-Silicon Infrastructure & Custom MCU

- Designed a custom MCU integrated with the IP to improve flexibility, testability, and debuggability.
- Integrated the custom MCU into a 32 GT/s x64 Advanced-Package UCIe PHY with SBD functionality.
- Built a dedicated compiler enabling post-silicon validation on ATE and rapid bug fixes via SW code.

RESEARCH

Seoul National University — Integrated System Design Lab Aug 2021 – Aug 2023

Graduate Researcher, advised by Prof. Deog-Kyoon Jeong — Seoul, South Korea

- Designed a 3.2 GHz integer all-digital PLL (ADPLL) achieving 857 fs RMS jitter at 7.6 mW through proportional –integral gain co-optimization.
- Designed and taped out a 14 nm FinFET Injection-Locked PLL (ILPLL) and its calibration circuitry.
- Performed post-silicon bring-up and characterization using oscilloscopes and spectrum analyzers.

EDUCATION

Seoul National University Sep 2021 – Aug 2023

M.S., Electrical and Computer Engineering

Sungkyunkwan University Mar 2015 – Aug 2021

B.S., Electronic and Electrical Engineering — GPA 4.28 / 4.5 (Summa Cum Laude)

PUBLICATIONS

- Y. Song, **K. Ha**, et al., "A −247.1 dB FoM, −77.9 dBc Reference Spur Ring-Oscillator-Based Injection-Locked Clock Multiplier with Multi-Phase-Based Calibration," *ESSCIRC*, 2022.

HONORS & AWARDS

- Rising Star Award (awarded to top early-career performers), Samsung Electronics (2025)
- Summa Cum Laude, Sungkyunkwan University (2021)
- Dean's List, Sungkyunkwan University (2020)
- National Science & Engineering Scholarship, KOSAF (2017)

TECHNICAL SKILLS

Expertise: PHY Design, Phase-Locked Loops, Mixed-Signal Integration, SerDes, RTL Design & Verification
Languages: SystemVerilog, UVM, Python, Tcl, MATLAB
Tools: Xcelium, Virtuoso, SPICE, PrimeTime, Design Compiler, Git